Data Sheet for SATA 2.0 Host Controller

iW-ASCDO-DS-01-R1.0

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1 Introduction

1.1 Purpose

This document describes the technical specification of high-speed serialized ATA 2.0 Host Controller. It includes the overall architectural description, functional specifications and interface definitions for the SATA Host Controller core.

1.2 Features

The following are the main features of the SATA Host Controller:

1.2.1 PHY Layer

The Transceiver available in the FPGA takes care of the Phy layer and following are the features of transceiver

- Converts 32 bit parallel data to differential Tx data and received Rx serial data to 32 bit parallel data
- Clock recovery from serial data
- 8B/10B encoding and decoding
- Byte ordering and word alignment
- OOB signaling detection and transmission

Following are some other features of Phy layer:

- Supports transmission and reception of COMRESET, COMINT and COMWAKE
- Supports speed negotiation.
- Supports reset controller for transceiver
- Device status and phy error status to Link layer

1.2.2 Link Layer

- **Frame Transmission**:
  - Initiation of the frame transmission
  - Link layer Flow control
  - Reception of FIS and envelope attachment to the FIS
  - Supports CRC on FIS
  - Supports transmit primitives scrambling
  - Reports good transmission and error status

- **Frame Reception**:
  - Acknowledges the readiness to receive a frame
  - Reception of 32 bit parallel data from the Phy Layer
  - Removes the envelope around the frame
  - Link layer Flow control
  - Supports CRC calculation and error detection
  - Supports received primitives descrambling
  - Reports good reception and error status

- **Primitives supported by Link Layer:**
  - $ALIGN_P$ - Phy layer control
  - $DMAT_P$ - DMA terminate
  - EOF_P - End of frame
  - $HOLD_P$ - Hold data transmission
  - $HOLDA_P$ - Hold acknowledge
  - R_ERR_P - Reception error
  - R_IP_P - Reception in Progress
  - R_OK_P - Reception with no error
  - R_RDY_P - Receiver ready
  - SOF_P - Start of frame
  - $SYNC_P$ - Synchronization
  - $WTRM_P$ - Wait for frame termination
  - X_RDY_P - Transmission data ready

- CONTp Primitive is not supported
- PMREQ_PP, PMREQ_SP, PMNAKP, PMACKP primitives are not supported

1.2.3 Transport Layer

- **FIS formation**:
  - Supports 32 bit AXI stream interface towards Application transmit interface
  - Formatting of the FISes and control information based on FIS type
  - Supports transport layer flow control
  - Reports good transmission and the error status

- **FIS decomposition**:
  - Supports 32 bit AXI stream interface towards Application transmit interface
  - Determines FIS type and distributes the FIS content
  - Supports transport layer flow control
  - Reports good reception and the error status

- **FIS Supported by Transport layer:**
  - Register FIS - 27h
  - Register FIS - 34h
  - DMA Activate FIS - 39h
  - DMA Setup FIS - 41h
  - Data FIS - 46h
  - PIO Setup FIS - 5Fh
  - Set Device Bits FIS - A1h

- BIST Activate FIS is not supported
- Support single device

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gated Array
SATA	Serial Advanced Technology Attachment
CRC	Cyclic redundancy check
DMA	Direct Memory Access
FIS	Frame Information structure
OOB	Out of band
SoC	System on chip
AHCI	Advanced host controller Interface

2 SATA Host Controller

2.1 Block Diagram

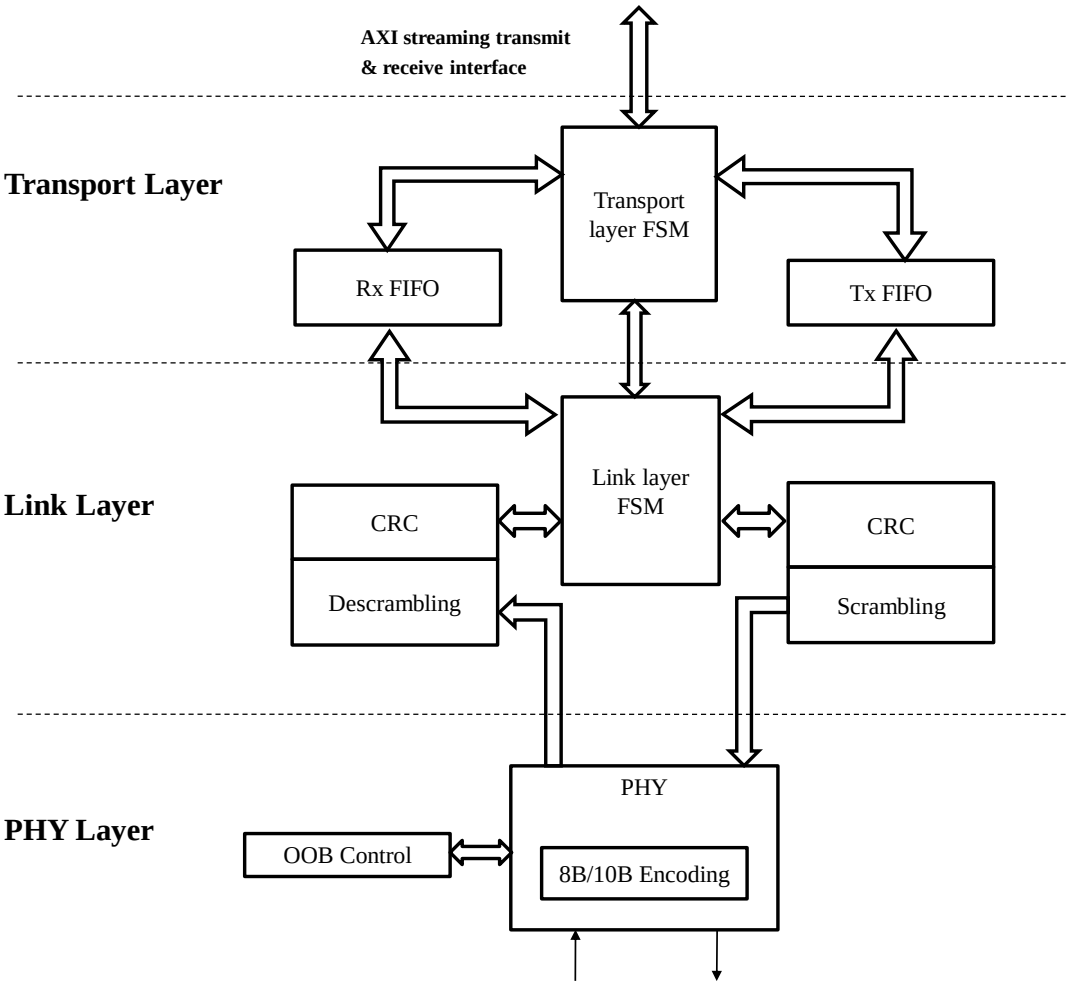

Figure 1: SATA Host Controller Block Diagram

The main blocks of SATA Host controller are given below.

- **PHY Layer:** The layer is responsible for generating the electrical signals that are transmitted and deciphering the received signals. The Phy layer serializes data to be transmitted and parallelizes received data. It controls the initialization of the SATA link using OOB signalling and Speed negotiations.
  - **OOB Control:** To establish a serial link between the host and device an initialization procedure is required. Before the link is up, the host and device communicates using OOB (Out of Band) signalling.
  - **Speed negotiation:** Speed negotiation is the process were the SATA link speed is configured. Host controller negotiates initially to the highest speed it supports. Reconfiguration controller IP will be used for speed negotiations.

- **Reset controller:** Some of the transceivers uses external Reset controller. External reset controller are used when the transceiver is not having the embedded reset controller.

- **Link Layer:** In SATA, data structures are referred to as frame information structures, so called FISes. This layer defines the protocol that transmits and receives packets (frames) that contains FISes.
  - **CRC generation:** The layer is responsible for performing error detection using the CRC algorithm. A CRC check sum is generated for each FIS that should be transmitted and each FIS is checked for errors by checking the received CRC check sum.
  - **Framing:** The main task for the Link layer is to encapsulate/unpack the FISes to/from frames by first sending/receiving a SOFp before the FIS, then calculate and send/receive the CRC value after the FIS and finally mark/identify the end of the frame by sending an EOFp.
  - **Scrambling/de-scrambling:** It is also responsible for scrambling transmitted payload data and descrambling received payload data.
  - **Link Layer FIFO Buffers:** FIFO will be used to store the FIS generated from Higher layer of the Design. These FISes will be fetched by link and framing will be done depending on the status of the host and device.

- **Transport Layer:** The transport layer module consist of the transport layer FSM and TX and RX FIFOs.
  During FIS formation, it receives payload data from user side using AXI transmit stream interface and defines the format and structure of the FISes and packs the control information and data into them. It also gathers FIS content from user data based on the type of FIS requested and responsible for placing the FIS content in the proper order. It request the link layer to initiate the frame transfer and transmits the FIS content to link layer and manages the transmit FIFO flow and does the flow control between the user side and link layer and reports good transmission and communicates the error status to user side
  During FIS reception, it is responsible for reception of the frames from the Link layer. Determines FIS type and distributes the FIS content to the locations indicated by the FIS type. It receives the acknowledgement from the link layer for reception of the data and manages the receive FIFO flow and does the flow control between the user side and link layer. It also interfaces with the user side using the AXI receive stream interface. It reports good reception and communicates the error status to user side

2.2 IO Signals

Table 2: System Interface IO Signals

Signal	I/O	Width	Description
sys_clk_i	I	1	Input system clock
ref_clk_i	I	1	Input reference clock. 150MHz clock used to as the reference clock to the transceiver
sys_reset_i	I	1	Input system reset.
SATA Interface			
tx_serial_data_o	O	1	PHY TX serial data to Device
rx_serial_data_o	O	1	PHY RX serial data to Device
Application layer Transmit Interface			
axi_user_clk_i	I	1	User clock for AXI TX and RX application layer transmit interface
axi_tx_data_i	I	32	Application layer transmit interface data bus.
axi_tx_tvalid_i	I	1	Application layer transmit interface data valid signal. When the axi_tx_tvalid_i and axi_tx_tready_o are high, indicates the valid data
axi_tx_tlast_i	I	1	Application layer transmit interface end of the frame signal. Asserted high with the last data of the burst
axi_tx_tready_o	O	1	Application layer transmit interface data ready signal. When the axi_tx_tvalid_i and axi_tx_tready_o are high, indicates the valid data
Application layer Receive Interface			
axi_rx_data_i	O	32	Application layer receive interface data bus.
axi_rx_tvalid_o	O	1	Application layer receive interface data valid signal. When the axi_rx_tvalid_o and axi_rx_tready_i are high, indicates the valid data
axi_rx_tlast_o	O	1	Application layer receive interface end of the frame signal. Asserted high with the last data of the burst
axi_rx_tready_i	I	1	Application layer receive interface data ready signal. When the axi_rx_tvalid_o and axi_rx_tready_i are high, indicates the valid data
Status Signals			
phy_link_up_o	O	1	Indicate that SATA link communication is established
phy_disparity_error_o	O	1	Phy RX 8B/10B disparity error status

Signal	I/O	Width	Description
phy_errdetect_o	O	1	Phy RX 8B/10B error detected status
crc_error_o	O	1	Asserted high when CRC error occurred in the frame received by the link layer
unknown_fis_o	O	1	Asserted high when unknown FIS is detected by the link layer
r_err_o	O	1	Bad/Unknown SATA FIS packet. WTRM primitive is received during read operation or R_ERR primitive is received at the end of write operation

3 Timing Diagram

The timing diagram of OOB Signaling is shown below.

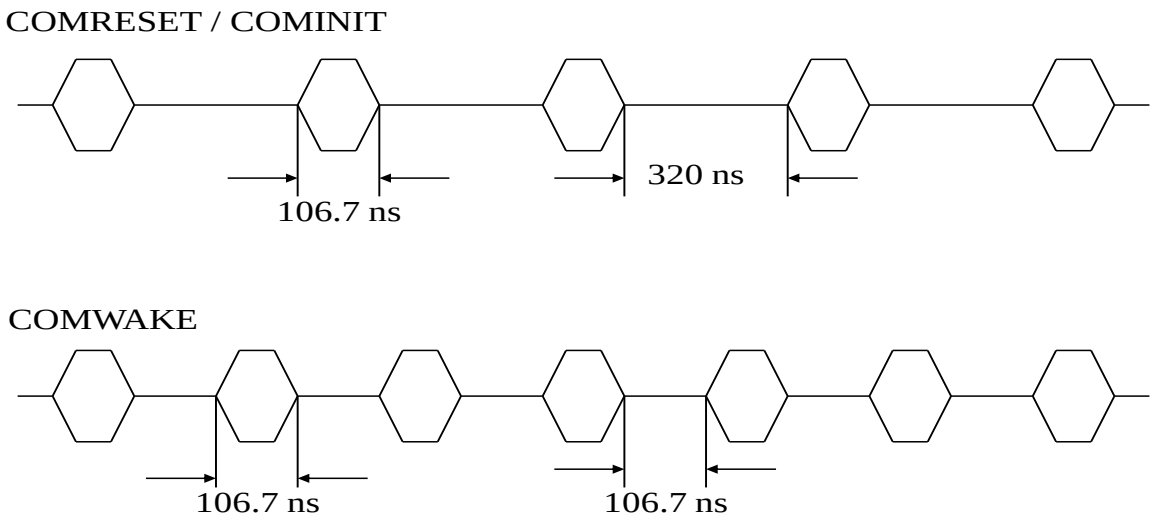

Figure 2: OOB Signal Timing

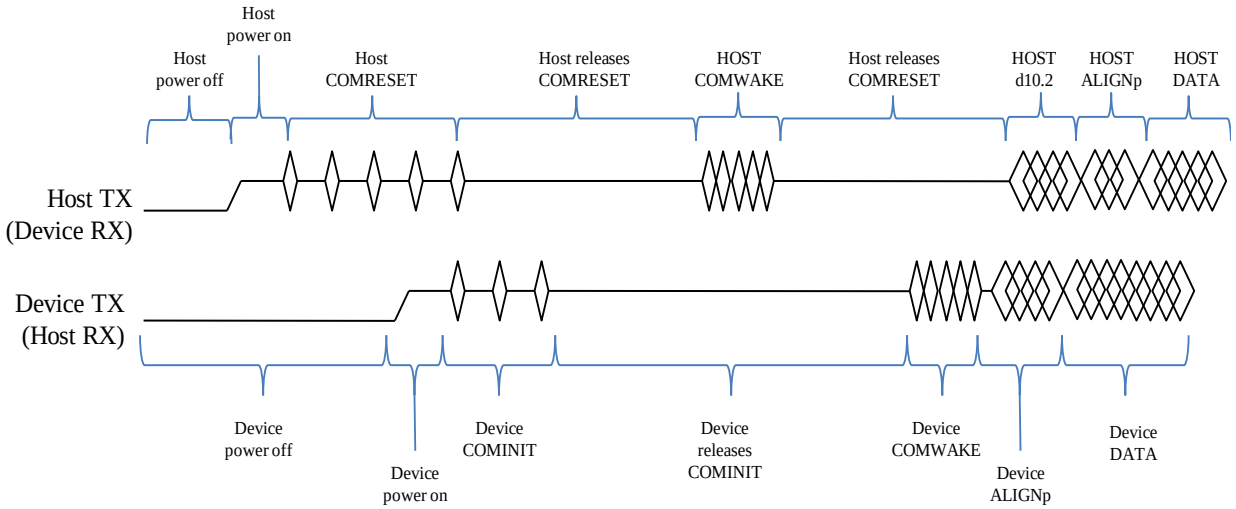

Figure 3: OOB Signaling

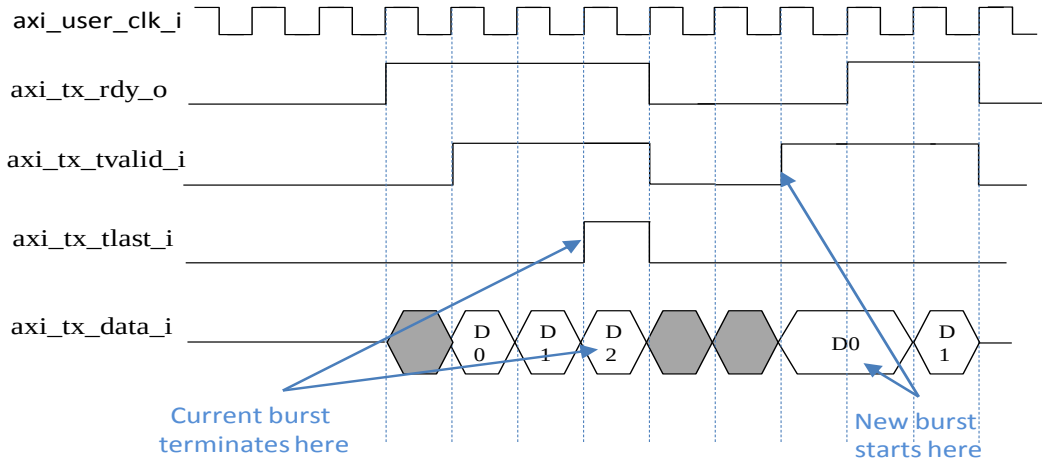

Figure 4: Typical AXI data transfer

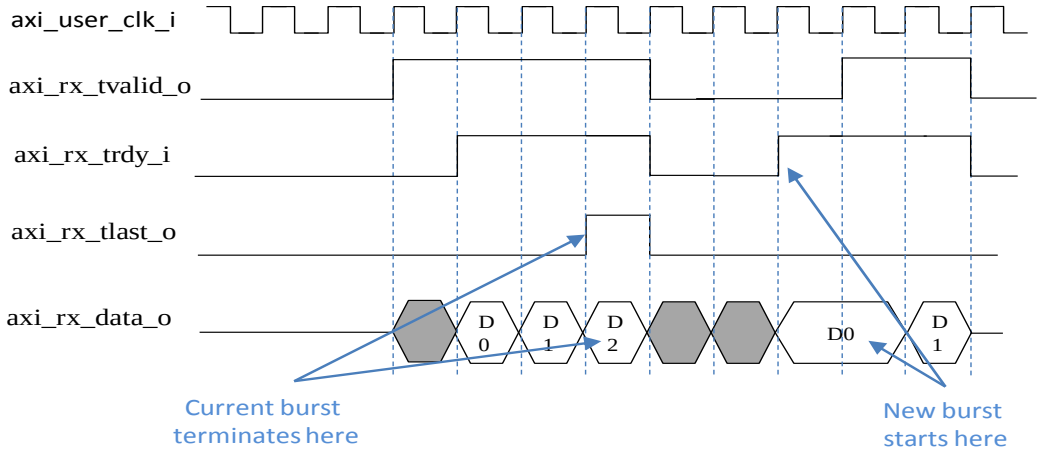

Figure 5: Typical AXI data reception

4 Implementation Results

The table below shows the utilization summary from the implementation of SATA Host Controller for FPGA devices.

Table 3: Device Utilization Summary for Altera Cyclone V

Logic Utilization	Used
Number of Combinational ALUTs	2233
Number of Logic Elements registers	1384
Transceiver Channels	1
PLL	1
Total Memory bits	150656

Table 4: Device Utilization Summary for Xilinx Kintex-7

Logic Utilization	Used
Number of Slice Registers	1196
Number of Slice LUTs	1180
Transceiver Channels	1
PLL	1
18K BRAM	2